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1.(Currently Amended) Compensation circuit (1-6) to compensate the nonlinear distortions of an A/D converter, ~~(1) (A/D: analog-to-digital)~~ comprising

- a signal input and

- a compensation circuit,

characterized by

a digital compensation circuit (2) having the signal input as the digital signal input to supply nonlinearly distorted digital data (x_n) from the A/D converter (1).

2.(Original) Compensation circuit according to Claim 1, comprising a coefficient determination system (5, 21) to determine adaptive coefficients (c_1, c_2, ..., c_K; $c_1(m)$, $c_2(m)$, ..., $c_K(m)$, $c_0(m)$) to compensate the nonlinear distortions in the compensation circuit (2).

3.(Original) Compensation circuit according to Claim 2, comprising a control device to turn on and off a configuration phase to determine the current adaptive coefficients (c_1, c_2, ..., c_K; $c_1(m)$, $c_2(m)$, ..., $c_K(m)$, $c_0(m)$).

4.(Original) Compensation circuit according to Claim 3, comprising a time monitoring device (C, T) to regularly turn on the configuration phase.

5.(Currently Amended) Compensation circuit according to claim 2, ~~one of Claims 2-4,~~ wherein the configuration circuit (2-6) ~~is designed to~~ generate

- an analog test signal (s(t)) having known test signal parameters (s_n; S_n), and has

- a connection to apply the analog test signal (s(t)) to the input of the A/D converter (1), and

- a connection to apply the test signal parameters (s_n; S_n) for subsequent processing in at least the coefficient determination system (5).

6. Compensation circuit according to Claim 5, comprising a test signal check device (4) which uses the test signal parameters (s_n) to extract and determine the signal map (S_n) of the analog test signal (s(t)) from the outputted digital compensated data (y_n) at the output of the compensation circuit (2).

7. Compensation circuit according to Claim 6, wherein the test signal check device (4) for determining a test frequency (F_t) has circuit elements (41, 42, 43, 45) such that a frequency band (-B, B) is maximized by a fundamental wave such that no significant harmonics are folded back at the output of the compensation circuit (2).

8. Compensation circuit according to Claim 7, wherein the test signal check device (4) has an I/Q-demodulator (41, 41a, 41b, I:in-phase, Q: quadrature phase), a Cordic circuit (43), and an amplitude estimation device (44a-44e).

9.(Currently Amended) Compensation circuit according to claim 6, ~~one of Claims 6-8,~~ comprising a subtracter (6) to form difference data (D_n) between digital data (y_n) outputted by the compensation circuit (2) and the signal map (S_n) as the measure of nonlinear distortions.

10.(Currently Amended) Compensation circuit according to claim 2, ~~one of Claims 2-9,~~ wherein the coefficient determination system (5, 21) has an exponentiation system (21) for data (x_n) outputted by the A/D converter (1) for the purpose of iteratively determining the adaptive coefficients by minimizing the square of the differences.

11.(Currently Amended) Compensation circuit according to claim 2, ~~one of Claims 2-10,~~ wherein the coefficient determination system (5, 21) and the compensation circuit (2) have a plurality (N) of uniform segments, each of which has a polynomial with coefficients ($c_1(m)$, $c_2(m)$, ..., $c_K(m)$, $c_0(m)$) assigned to it, wherein the compensation circuit has an adder (23) to sum the number of the plurality of segments.

12. Compensation circuit according to Claim 11, wherein the compensation circuit (2), and specifically, the coefficient determination system (5) has a coefficient memory system ($52,52_0$, ..., 52_{N-1}) to store the N coefficient sets with (K+1) coefficients each for application in the compensation circuit (2).

13.(Currently Amended) Compensation circuit according to claim 11, ~~Claims 11 or 12,~~ comprising an index determination device (51) to determine an index (m) for the current coefficient set corresponding to the plurality of segments (m = 0, 1, 2, ..., N-1) from input data (x_n) of the compensation circuit (2).

14.(Currently Amended) Compensation circuit according to claim 2, ~~one of Claims 2-13,~~ comprising a look-up table (52_0, 52_1, ... 52_{N-1}) to provide the adaptive coefficients ($c_1(m)$, $c_2(m)$, ..., $c_{N-1}(m)$, $c_0(m)$).

15. Compensation circuit according to Claim 14, wherein the look-up table (52) has a memory location number (N) equal to the signal resolution of the data to be compensated (x_n).

16.(Currently Amended) Compensation circuit according to claim 11 ~~one~~ of Claims 11-15, wherein the coefficient determination system (5, 21) is designed to address the adaptive

17. A/D converter circuit, comprising

- an A/D converter (1) and
- a compensation system for compensating the nonlinear distortions of the A/D converter (1),

characterized in that the compensation system, specifically, a compensation circuit (2-6) is designed according to a foregoing claim as a digital, nonlinearly compensating compensation circuit (2) and the compensation circuit (2) is connected after the A/D converter (1).

18. Method to compensate a nonlinear distortion of an A/D converter (1), wherein

- nonlinearly distorted data(x_n) are outputted by the A/D converter (1), and
- the nonlinearly distorted output data (x_n) are fed to a compensation circuit (2), specifically a compensation circuit (2-6) according to a foregoing claim, to compensate the nonlinear distortion.

19. Method according to Claim 18, wherein the nonlinear compensation is implemented in the compensation circuit (2) using adaptive coefficients (c_1, c_2, ..., c_K; $c_1(m)$, $c_2(m)$, ..., $c_K(m)$, $c_0(m)$).

20. Method according to Claim 19, wherein

- an analog test signal (s(t)) is generated and fed to the analog input of the A/D converter (1), and
- the adaptive coefficients (c_1, c_2, ..., c_K; $c_1(m)$, $c_2(m)$, ..., $c_K(m)$, $c_0(m)$) for use in the compensation circuit (2) are determined using known test signal parameters (s_n; S_n) from the digital data (x_n, y_n) outputted for the analog test signal (s(t)) by the A/D converter (1).

CLAIMS-21-22 HAS BEEN CANCEL